

**107550094****JC05 Rec'd PCT/PTO 21 SEP 2005****PATENT APPLICATION**

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

In re application of: )  
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                             )  
 HANSEN et al.           ) Group Art No. TBA  
                             )  
 Serial No: TBA          ) Examiner: TBA  
                             )  
 Filed: Herewith         ) Docket No. 006559.00009

For: *LIST OUTPUT VITERBI DECODER  
WITH BLOCKWISE ACS AND TRACEBACK*

**INFORMATION DISCLOSURE STATEMENT**

Commissioner of Patents  
 U.S. Patent and Trademark Office  
 Customer Service Window  
 Randolph Building  
 401 Dulany Street  
 Alexandria, VA 22314

Sir:

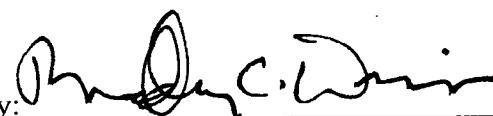
Pursuant to 37 C.F.R. §1.56 and in compliance with 37 C.F.R. §1.97, Applicants submit herewith Form PTO-1449 identifying information for consideration by the Examiner. Copies of the cited documents were provided with the International Search Report.

If the Patent and Trademark Office determines that a fee is required, please charge our Deposit Account No. 19-0733.

Respectfully submitted,

**BANNER & WITCOFF, LTD.**Date Sept. 21, 2005

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ALL REFERENCES CONSIDERED EXCEPT WHERE LINED THROUGH. /S.H./

USPTO Form 1449 U.S. Department of Commerce Patent and Trademark Office <b>INFORMATION DISCLOSURE</b> <b>CITATION</b> Sheet 1 of 1			Attorney Docket No. <b>10/550094</b>		Serial No. TBA	
			Applicant(s): HANSEN et al			
			Filing Date: September 21, 2005			Group: TBA
<b>U.S. PATENT DOCUMENTS</b>						
Examiner Initial	Patent No.	Date	Name	Class	Subclass	Filing Date (if appropriate)
<b>FOREIGN PATENT DOCUMENTS</b>						
Examiner Initial	Document No.	Date	Country	Class	Subclass	Translation
						YES
	GB 2 305 827 A	16 April 1997	Great Britain			
<b>OTHER DOCUMENTS</b> (including Author, Title, Date, Pertinent Pages, etc.)						
	CZAJA et al.: "Variable data rate Viterbi decoder with modified LOVA algorithm", TENCON '95, PROCEEDINGS OF THE IEEE REGION 10 INTERNATIONAL CONFERENCE ON MICROELECTRONICS AND VLSI, Hong Kong, November 6-10, 1995, pages 472-475. XP010160164.					
	BOUTILLON et al.: "VLSI architectures for the MAP Algorithm", IEEE TRANSACTIONS ON COMMUNICATIONS, vol. 51, no. 2, February 2003, pages 175-185, XP001164390.					
	FETTWEIS et al.: "Feedforward Architectures for Parallel Viterbi Decoding", JOURNAL OF VLSI SIGNAL PROCESSING SYSTEMS FOR SIGNAL, IMAGE, AND VIDEO TECHNOLOGY, vol. 3, no. 1 / 2, June 1, 1991, pages 105-119, XP00228897.					
	SEARCH REPORT, mailed March 9, 2004					
EXAMINER /Syed Haider/ (12/14/2010)				DATE CONSIDERED 12/14/2010		
<small>*EXAMINER: Initial if reference considered, whether or not citation is in conformance with MPEP 609. Draw line through citation if not in conformance and not considered. Include copy of this form with next communication to Applicant.</small>						

ALL REFERENCES CONSIDERED EXCEPT WHERE LINED THROUGH. /S.H./